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10/659,701	09/11/2003	Pavel Peleska	449122062100	4756

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EXAMINER	
ASSESSOR, BRIAN J	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,701	PELESKA ET AL.	
	Examiner	Art Unit	
	Brian J. Assessor	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-18,20 and 21* is/are rejected.

7)☒ Claim(s) *7,8 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 9, 12, 15-18, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Horst (5,838,894).

As per claim 1, Horst teaches:

A method for synchronizing redundant processing units which are clocked synchronously or asynchronously, comprising:

providing an identical instruction sequence to each of the redundant processing units; (Horst column 74, lines 22-25)

assigning a module to each of the processing units; (figure 1a, elements 14a and 14b)

monitoring transactions that are external to the processing units via the modules; (Horst column 74, lines 40-42; the comparison would be done outside the processing by the module units.)

achieving synchronization by placing the processing units in a wait state via the modules until the processing units have reached a current transaction. (Horst column 75, line 64 – column 76, line 16; the FIFOs within the router modules maintain the

synchronization of the processors by delaying (wait state) the instructions until both processors receive the instruction.)

As per claim 2, Horst teaches:

The method according to claim 1, further comprising transferring parameters by the modules via connections for synchronization of the processing units which are characteristic of the transactions. (Horst column 75, line 64 – column 76, line 16; the FIFOs contain pull and push counters which are set to ensure synchronization of the CPU execution of the instructions.)

As per claim 3, Horst teaches:

The method according to claim 2, wherein executing a read transaction comprises:

leaving a processing unit in the wait state until arrival of data to be read via the module associated with the respective processing unit; (Horst column 75, line 64 – column 76, line 16; the FIFOs within the router modules maintain the synchronization of the processors by delaying (wait state) the instructions until both processors receive the instruction.)

sending the parameters of the read transaction to the module connected most directly with a transaction destination; (Horst column 5, lines 57-64; the routers (modules) receive and send messages (parameters) to and from the processing units and the I/O devices.)

at the module connected most directly to the transaction destination, receiving and comparing the parameters from other modules and locally created parameters; (Horst column 74, lines 40-43)

executing the read transaction and distributing the read data to the modules upon determining that the parameters match; (Horst column 7, lines 30-36; the CPU will execute the instruction after the comparison result shows no errors in the instruction.)

at each module, forwarding the read data to the assigned processing unit and enabling continuation of instruction processing. (Horst column 5, lines 57-64; the routers (modules) receive and send messages (parameters) to and from the processing units.)

As per claim 4, Horst teaches:

The method according to claim 3, further comprising executing a data comparison to check the data integrity (Horst column 5, lines 36-43; CRC check) by reading data areas from main memories at regular intervals or on request and comparing the parameters of the read transactions, the comparison being made by at least one of the modules. (Horst column 74, lines 40-43; comparison of duplex processor outputs.)

As per claim 5, Horst teaches:

The method according to claim 2, wherein the executing a write transaction comprises:

leaving a processing unit in the wait state until a write process is completed via the module associated with that processing unit; (Horst column 75, line 64 – column 76, line 16; the FIFOs within the router modules maintain the synchronization of the processors by delaying (wait state) the instructions until both processors receive the instruction.)

sending the parameters of the write transaction to the module connected most directly with a transaction destination; (Horst column 5, lines 57-64; the routers (modules) receive and send messages (parameters) to and from the processing units and the I/O devices.)

at the module connected most directly to the transaction destination, receiving and comparing the parameters from other modules and locally created parameters; (Horst column 74, lines 40-43)

executing the write transaction and acknowledging the write process to the modules upon determining that the parameters match; (Horst column 7, lines 30-36; the CPU will execute the instruction after the comparison result shows no errors in the instruction.)

at each module, enabling continuation of instruction processing for the assigned processing unit. (Horst column 5, lines 57-64; the routers (modules) receive and send messages (parameters) to and from the processing units.)

As per claim 6, Horst teaches:

The method according to claim 2, wherein external events are buffered, whereby stored external events are called in a special operating mode of the processing units for processing by at least one execution unit of the processing units and the processing unit enters the operating mode in response to fulfillment of a condition that is pre-specified by instructions or fixed in advance, and continuation of instruction execution is delayed by the modules until the processing units have ended the special operating mode. (Horst column 6, line 61 – column 7, line 15; interrupt events are caused by an instruction packet sent to the processors, causing the processor to interrupt normal operation and go into an interrupt mode. These interrupts wait for the current I/O instruction to finish before executing and therefore are buffered during the current I/O instruction.)

As per claim 9, Horst teaches:

The method according to claim 1, further comprising providing a direct memory access for transmission of data from the memory to an input/output module through initiation of direct memory access by jobs generated by a processing unit being transferred to the input/output module by entry into a register. (Horst column 18, lines 40-44)

As per claim 12, Horst teaches:

The method according to claim 2, wherein fault handling is initiated by a module linked most directly to a transaction destination if a deviation from the parameters of the

other modules and locally generated parameters are established. (Horst column 21, lines 27-44; the interface units compare the states and once the processing units fall out of sync an error signal is sent out for correction.)

As per claim 15, Horst teaches:

The method according to claim 2, wherein failures of individual processing units are detected such that for a transaction beginning with an earliest availability of the parameters at the module of a processing unit, error processing is initiated for processing units with parameters that do not arrive or arrive after expiry of a pre-specified time. (Horst column 42, lines 61-63)

As per claim 16, Horst teaches:

The method according to claim 1, wherein at least one of the following transactions are used by the modules for synchronization of the processing unit:

non-cacheable memory transactions relating to a local memory assigned to a relevant processing unit,

input/output transactions for input/output modules, (Horst column 4, lines 47-54; I/O packets are sent during the synchronization of the processors.)

memory-mapped input/output transactions for external registers, and

non-cacheable memory transactions relating to a common memory of processing units.

As per claim 17, Horst teaches:

The method according to claim 2, wherein at least one of the following parameters of transactions are transferred by the modules via connections for synchronization of the processing units:

input/output addresses, (Horst column 4, lines 47-54; I/O packets are sent during the synchronization of the processors, therefore I/O addresses would be used for transmission of the packets.)

memory addresses,

data to be transferred,

type of transaction,

a signature formed from the input/output addresses,

the memory addresses,

the data to be transferred, and

the type of transaction.

As per claim 18, Horst teaches:

An arrangement to synchronize synchronously or asynchronously clocked processing units of redundant data processing systems, comprising:

at least two processing units for processing identical instruction sequences; (Horst column 74, lines 22-25)

peripherals assigned to each of the processing units for saving and/or exchanging data; (Horst column 6, lines 30-34)

peripherals jointly usable by the processing units for saving and/or exchanging data; (Horst column 6, lines 30-34)

modules assigned to each of the processing units, (figure 1a, elements 14a and 14b) the modules including a first unit to monitor transaction, (Horst column 74, lines 40-42; the comparison would be done outside the processing by the module units.) a second unit to stop the associated processing unit until a current transaction has been reached by the processor units, and a third unit to transfer parameters of the transactions to other modules. (Horst column 75, line 64 – column 76, line 16; the FIFOs within the router modules maintain the synchronization of the processors by delaying (wait state) the instructions until both processors receive the instruction.)

As per claim 20, Horst teaches:

The arrangement in accordance with claim 18, wherein the modules include a fourth unit to synchronize the processing units, based on the following transactions:

non-cacheable memory transactions relating to a local memory assigned to a relevant processing unit,

input/output transactions for input/output modules, (Horst column 4, lines 47-54; I/O packets are sent during the synchronization of the processors.)

memory-mapped input/output transactions for external registers, and

non-cacheable memory transactions relating to a common memory of processing units.

As per claim 21, Horst teaches:

The arrangement in accordance with claim 18, wherein the modules include a fifth unit to form the following parameters representative for transactions:

input/output addresses, (Horst column 4, lines 47-54; I/O packets are sent during the synchronization of the processors, therefore I/O addresses would be used for transmission of the packets.)

memory addresses,

data to be transferred,

type of transaction, and

a signature formed from at least one of the input/output addresses, the memory addresses, the data to be transferred, and the type of transaction.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horst (5,838,894) in view of

http://www.computing.dcu.ie/~ray/NewCA104/DMABig.pdf (herein referred to as DMA Power Point)

As per claim 10:

Horst fails to explicitly disclose a method describing the process through which it does the DMA transmissions. The DMA Power Point clearly discloses a method in which the steps to DMA are broken down and simply explained.

It would have been obvious to a person of ordinary skill in the art at the time of invention to include the DMA process as taught by the DMA Power Point in order to control DMA transmissions. This would have been obvious because the DMA Power Point clearly teaches that this process of DMA transfers is known in the art and would have been used during DMA transmissions.

The method according to claim 1, further comprising providing a direct memory access for transmission of data from an input/output module into memory, such that a descriptor generated by an input/output module is stored in memory and is read out by the processing units with a polling procedure, (DMA Power Point, page 6; CPU sets up the DMA machine.)

reading a register in one of the modules by the processing units causing no more write transactions in the memory by input/output modules, (DMA Power Point, page 7; CPU stops to allow DMA to control the bus.)

writing a last of the write transactions sent by the input/output modules by the modules into the memory of the processing units, (DMA Power Point, page 7; the pending CPU instructions are stored when the CPU is halted.)

reading a memory location in the memory of the processing units for which a value shows completion of a direct memory access, (DMA Power Point, page 7; the DMA machine returns control of the bus to the CPU.)

reading or writing to the register or another register to permit write access to the memory by the I/O units. (DMA Power Point, page 7; CPU resumes control of the bus.)

As per claim 11:

Horst fails to explicitly disclose a method describing the process through which it does the DMA transmissions. The DMA Power Point clearly discloses a method in which the steps to DMA are broken down and simply explained.

It would have been obvious to a person of ordinary skill in the art at the time of invention to include the DMA process as taught by the DMA Power Point in order to control DMA transmissions. This would have been obvious because the DMA Power Point clearly teaches that this process of DMA transfers is known in the art and would have been used during DMA transmissions.

The method according to claim 1, further comprising providing a direct memory access for transmission of data between input/output module and a memory,

reading a register in one of the modules by the processing units causing no more read transactions by the input/output modules permitted in the memory, (DMA Power Point, page 7; CPU stops to allow DMA to control the bus.)

storing a descriptor generated by the processing units in the memory which can be read out by one or more input/output modules with a polling procedure, (DMA Power Point, page 6; the starting address of the DMA access is stored in a register.)

reading or writing the register or another register to permit read access to the memory by the I/O units, (DMA Power Point, page 6; the control information for which I/O devices have access to the bus is stored in a register.)

reading a memory location in the memory of one or more input/output modules, for which the value indicates the beginning of a direct memory access. (DMA Power Point, page 6; the DMA starts reading from the start address.)

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horst (5,838,894) in view of Bissett (20020026604).

As per claim 13:

Horst does not explicitly disclose a method wherein the fault handling stops the transaction to be executed and starts a routine for detection of the faulty unit, the isolation and recovery of which to re-establish the synchronicity.

In page 4, paragraphs 0049-0050; Bissett clearly discloses a method for re-synchronizing the processing units when an error occurs. It would have been obvious to a person skilled in the art a the time of invention in order to create a more fault tolerant synchronization method. This would have been obvious because Bissett clearly

teaches that the above process is better suited for creating a more fault tolerant and resilient computer system. (Bissett page 1, paragraph 0015 – page 2, paragraph 0016)

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horst (5,838,894) in view of Griffin (6,928,583).

As per claim 14:

Horst does not explicitly disclose a method wherein with N available processing units the error handling makes an N-M (M<N) out of N majority decision and deactivates a divergent processing unit. In column 10, lines 16-25; Griffin clearly discloses a method wherein a majority decision is made among processing units in order to make a decision.

It would have been obvious to a person of ordinary skill in the art at the time of invention to include the system as taught by Griffin in order to create a system that can detect and determine the presence of a faulty processing unit. This would have been obvious because Griffin clearly teaches that the above method is better suited for fault tolerant processing systems working in synchronization. (Griffin column 1, lines 38-52)

Allowable Subject Matter

Claims 7, 8, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Assessor whose telephone number is (571) 272-0825. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER

BA